Claims 2-4 and 6-8 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including the base claim and any intervening claims.

II. CLAIMS 1 AND 5 ARE NOT ANTICIPATED BY SNYDER BECAUSE SNYDER FAILS TO DISCLOSE UTILIZING A DIGITAL DIFFERENTIAL ANALYZER TO GENERATE THE CLAIMED SYNCHRONIZATION SIGNAL

Claims 1 and 5 stand rejected under 35 U.S.C. § 102(b) as being unpatentable over Snyder (USP No. 5,422,914). Applicants respectfully submit that neither claim 1 nor claim 5 are anticipated by Snyder for the following reasons.

With regard to the pending claims, both claims 1 and 5 recite a digital differential analyzer utilized to ***generate a synchronization signal having a frequency proportional to a ratio of a first clock rate and a second clock rate***, wherein the first clock rate corresponds to, for example, the system clock (M), and the second clock rate corresponds to, for example, the communications clock (N). In the given example, the system clock (M) is faster than the communications clock (N).

In accordance with the present invention, the digital differential analyzer receives both the M and N clock signals as input signals and generates the aforementioned synchronization signal. In other words, the digital differential analyzer functions to output N enabling signal values every M clock cycles (where the N enabling signals are spread out evenly as possible over the M clock cycles).

Continuing, the data to be transmitted is read into a plurality of registers at the system clock rate (M), and then read out of registers utilizing the synchronization signal. In other words, the data is read out of the registers at a frequency equal to that of the

synchronization signal (i.e., the ratio of M:N). As detailed in the specification, the plurality of registers function as a data buffer during the foregoing synchronization of the data to the communications clock (N).

Turning to the cited prior art, it is respectfully submitted that, at a minimum, Synder does not disclose or suggest the claimed digital differential analyzer or the generation or use of the claimed synchronization signal. More specifically, as is known and as stated above, a digital differential analyzer is a sequential circuit which generates an output signal having a frequency corresponding to the ratio of the frequency of a first clock signal and the frequency of a second clock signal. The first clock signal and the second clock signal are received as inputs to the digital differential analyzer (the output of the digital differential analyzer corresponds to the claimed synchronization signal). Contrary to the assertion set forth in the pending rejection, the control circuit 34 of Synder does not correspond to the claimed digital differential analyzer, nor does the control circuit 34 produce a signal corresponding to the claimed synchronization signal.

Referring to Fig. 4 of Synder and the corresponding description set forth on col. 5, lines 4-15, the control circuit 34 generates two signals, namely, the LATCH/FORWARD signal and the PASS/MASK signal. However, as expressly stated by Synder, **both** of these signals have a frequency equal to the quotient of (1) the clock frequency of the slower device and (2) M, or the quotient of the (1) clock frequency of the faster device and (2) N, where N corresponds to the frequency of the faster device and M corresponds to the frequency of the slower device. Thus, both the LATCH/FORWARD signal and the PASS/MASK signal have frequencies corresponding

to either the fast device or the slow device (as is shown in Fig. 2). As such, the control circuit 34 does not produce a signal having a frequency corresponding to the ratio of the frequency of the first and second clock signals. Accordingly, the control circuit 34 of Synder does not correspond to the claimed digital differential analyzer. Nor does the control circuit 34 generate a signal corresponding to the synchronization signal.

Moreover, Synder also fails to disclose reading the data to be transmitted into a plurality of registers at the first clock rate system, and then reading the data out of registers utilizing the synchronization signal, as recited by claims 1 and 5. In contrast to the claimed invention, referring to Fig. 4 of Synder, Synder discloses outputting the signal associated with the processor utilizing the signal LATCH/FORWARD, and outputting the signal associated with the bus utilizing the signal PASS/MASK. However, as stated above, the LATCH/FORWARD signal and the PASS/MASK signal correspond to the frequency associated with the fast device and the slow device, respectively. Neither signal represents a ratio of the clock frequencies utilized by the fast and slow device. Thus, Synder also fails to satisfy the claim limitation requiring the data to be read out of the registers utilizing the synchronization signal.

According, as anticipation under 35 U.S.C. § 102 requires that each and every element of the claim be disclosed in a prior art reference, ***Akzo N.V. v. U.S. Int'l Trade Commission***, 808 F.2d 1471 (Fed. Cir. 1986), and at a minimum, Synder fails to disclose the claimed digital differential analyzer, or the synchronization signal, or the use of the synchronization signal to read out data from the registers, it is clear that Snyder does not anticipate either claim 1 or claim 5.

As such, it is respectfully requested that the pending rejection of claims 1 and 5 in view of Synder be withdrawn.

III. CONCLUSION

Having fully and completely responded to the Office Action, Applicants submit that all of the claims are now in condition for allowance, an indication of which is respectfully solicited.

If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

Respectfully submitted,

McDERMOTT, WILL & EMERY

Date: 3/20/01

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